

Introduction of SIGLEAD

For Year 2011
Ver. 1.2

SIGLEAD Inc.
www.siglead.com , info@siglead.com

1. SIGLEAD Profile

Company Overview / Management Team / Organization
Core Competence / Business Territory

Company Overview

Name	SIGLEAD Inc.
Headquarter	Yokohama-city Kanagawa-ken, Japan
President	Atsushi Esumi (President & CEO)
Web Site	http://www.siglead.com/eng/
Establishment	February 5, 2007
Paid-in Capital	695.1 million Yen
Shareholders	Co-founders, Venture Capital
Executives	Atsushi Esumi, Ichiro Myochin Kanji Sakae, Kunihiro Kawahara
Total Members	14
Business	<ul style="list-style-type: none"> ➤ Solid State Drive (SSD) controller LSI ➤ Hard Disk Drive (HDD) signal processing LSI ➤ NAND flash memory analyzer system ➤ Signal processing IP ➤ FPGA board



Management Team

- Atsushi Esumi (president & CEO)

Graduate school of Kobe University, Toshiba, ROHM Co., Ltd.

Long term experience on R&D of HDD signal processing and development Of HDD R/W channel LSI. Also be responsible for CTO.

- Ichiro Myochin (executive, Marketing & Management)

NEC IC Micon Systems, Mikasa Trading Co., Ltd. Holding the experience of ASIC development and sale. In 2004, joined in System Solution Inc. as a executive, successfully achieved the establishment of the company.

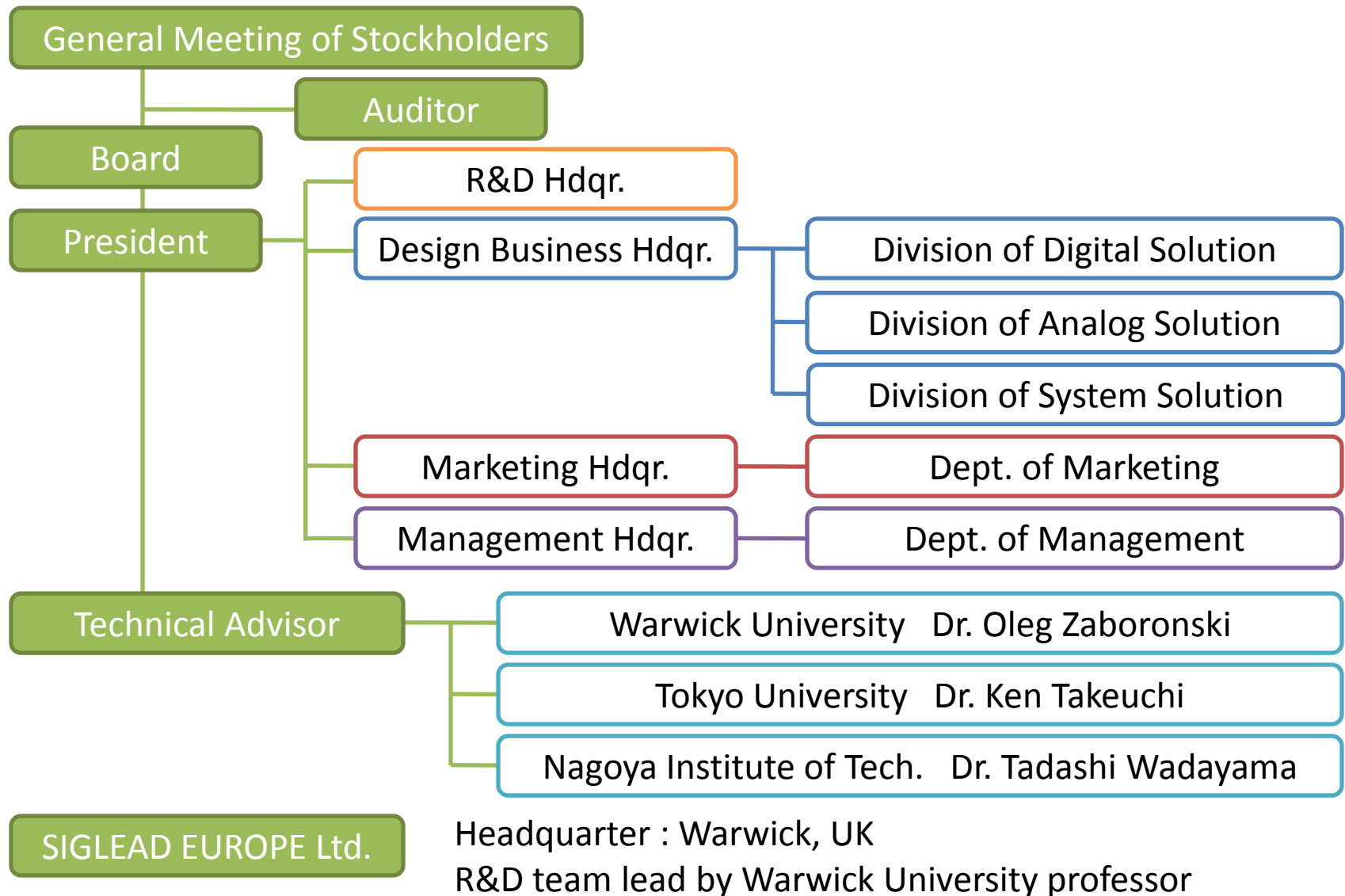
- Kanji Sakae (executive, part time)

Co-founder & president of PeerMe Inc. In SIGLEAD, he plays the role of CFO.

- Kunihiro Kawahara (executive, part time)

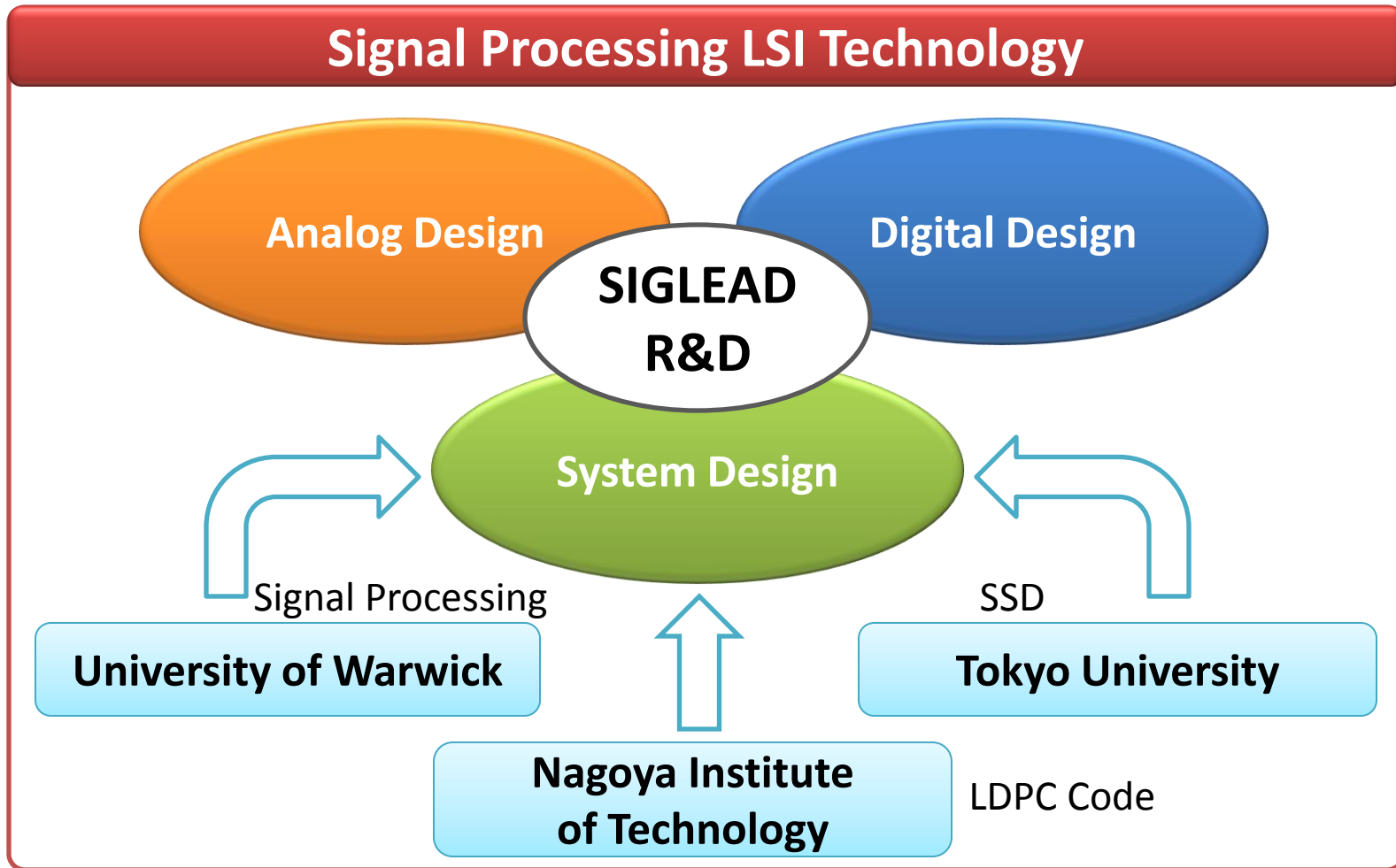
President & CEO of Solid Alliance Inc. In SIGLEAD, he is responsible for marketing, finance and public relationship.

Organization

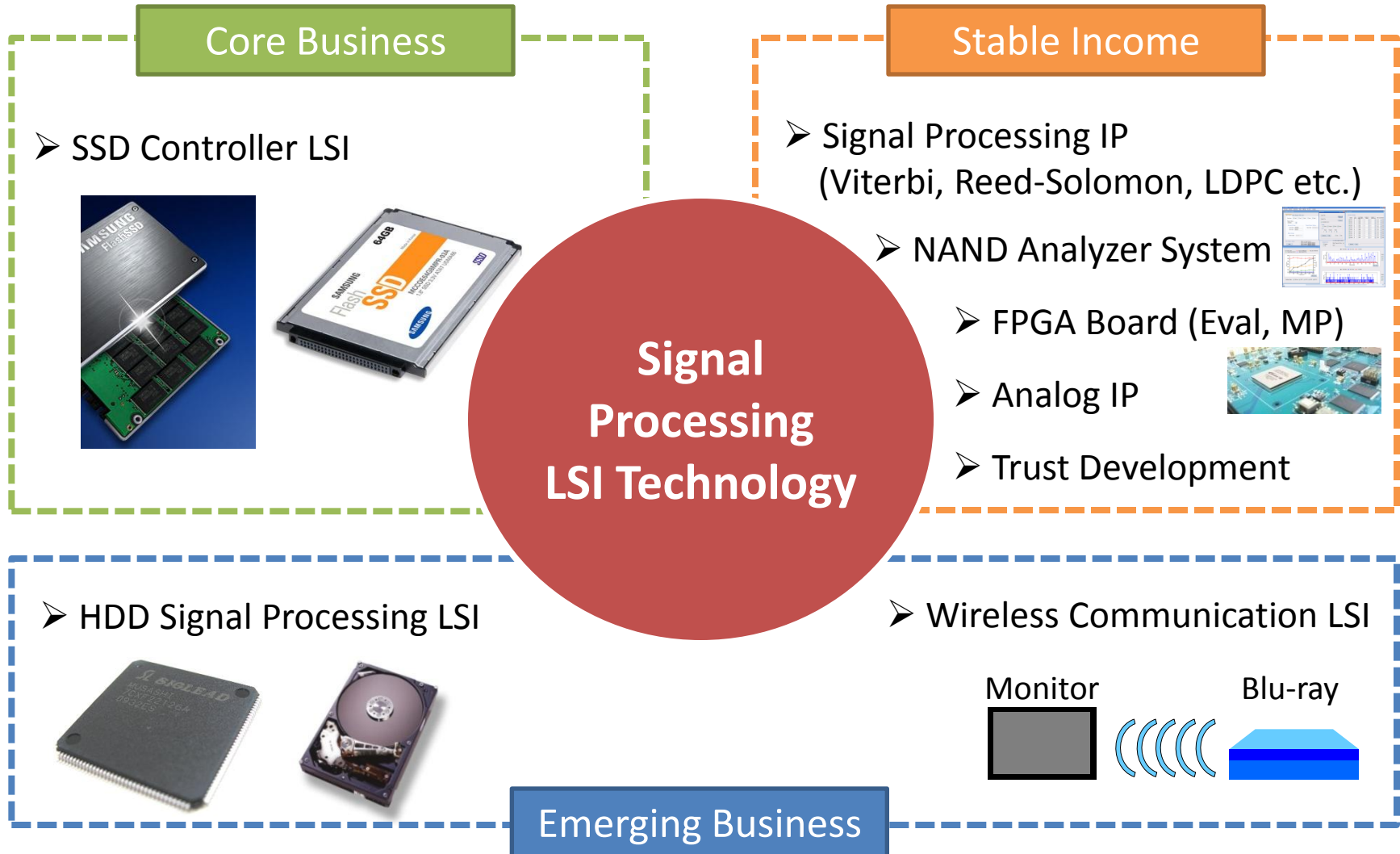


Core Competence

SIGLEAD's R&D and the collaboration with University ensures the best technology in the world.



Business Territory



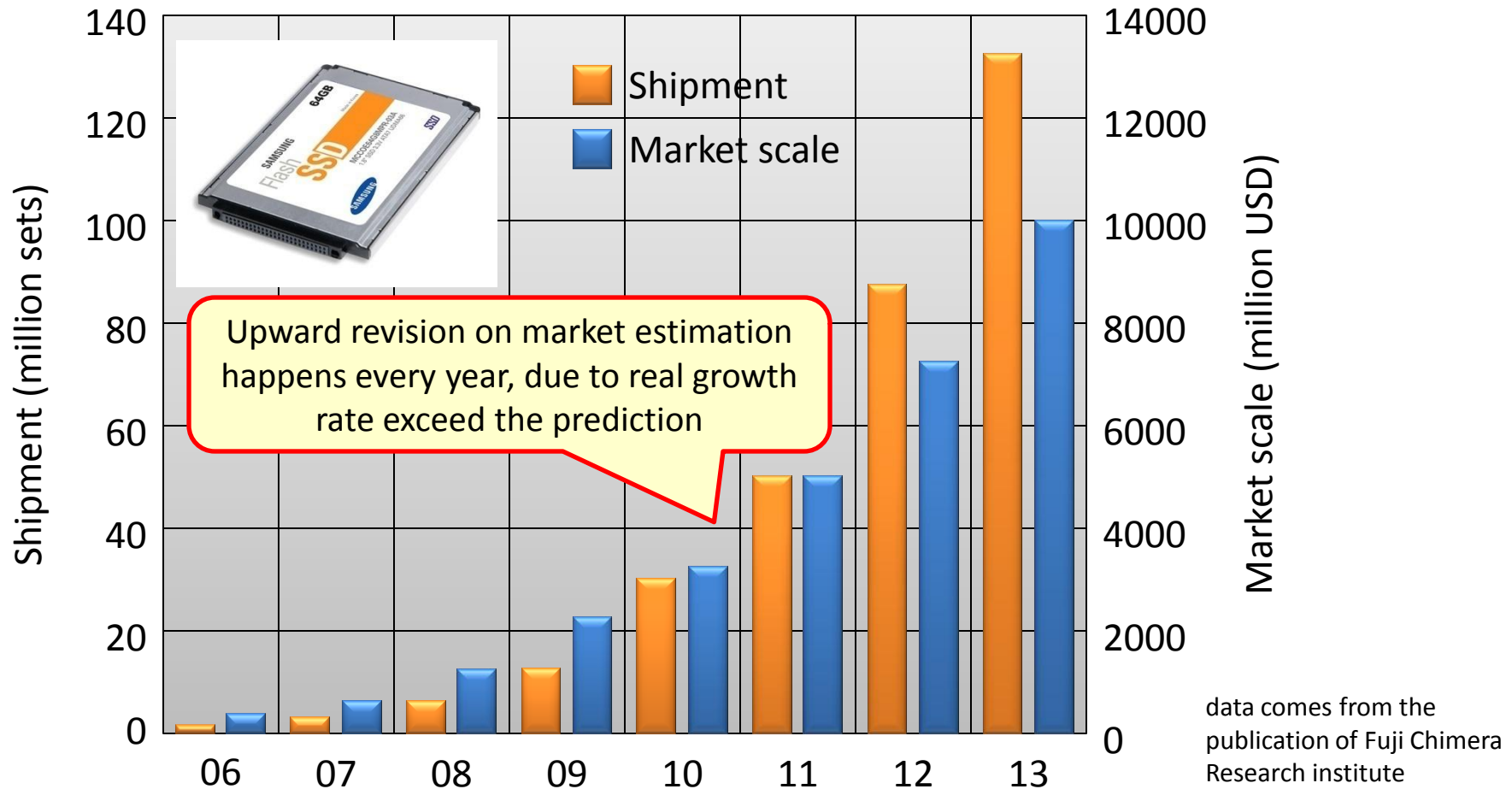
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2. SSD Controller LSI

Market / SSD Developing Trends / Original Technology
LSI Overview / Service Options

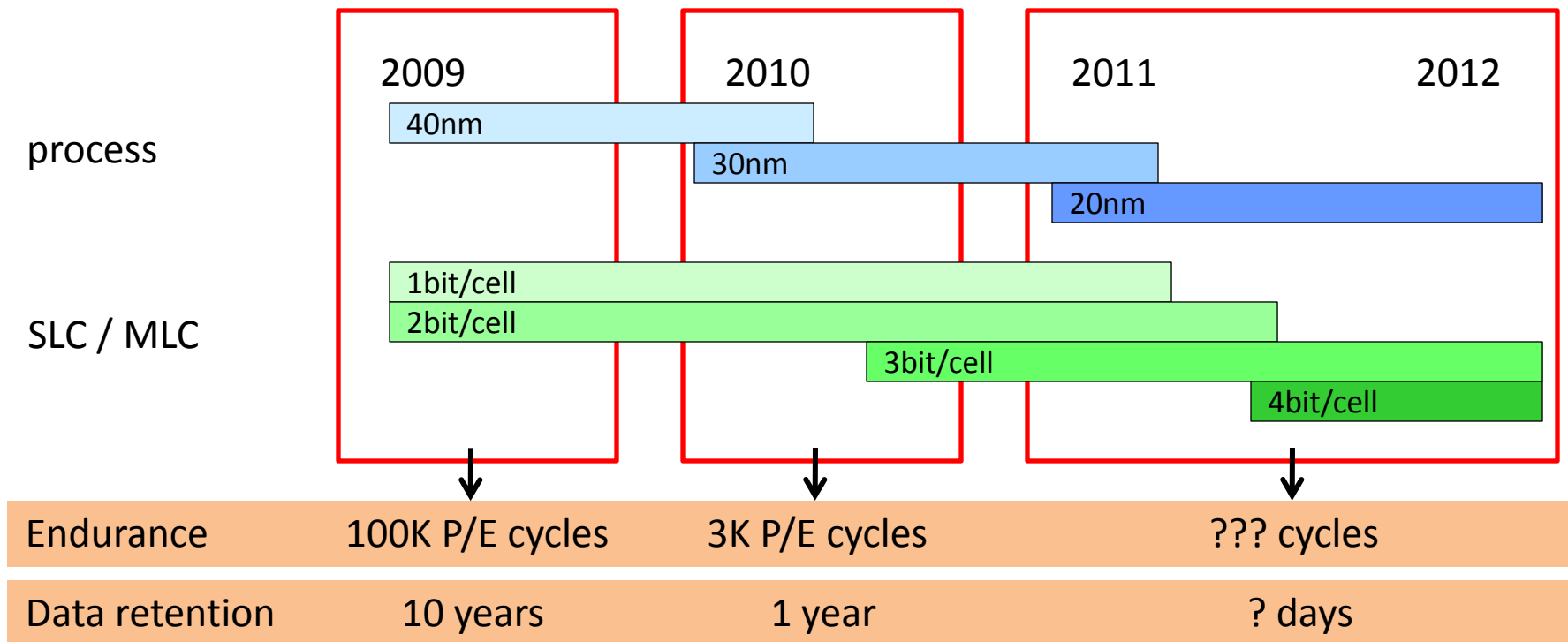
Market

SSD market growth believed to continue in the future



SSD's Developing Trends 1 (NAND Flash Memory)

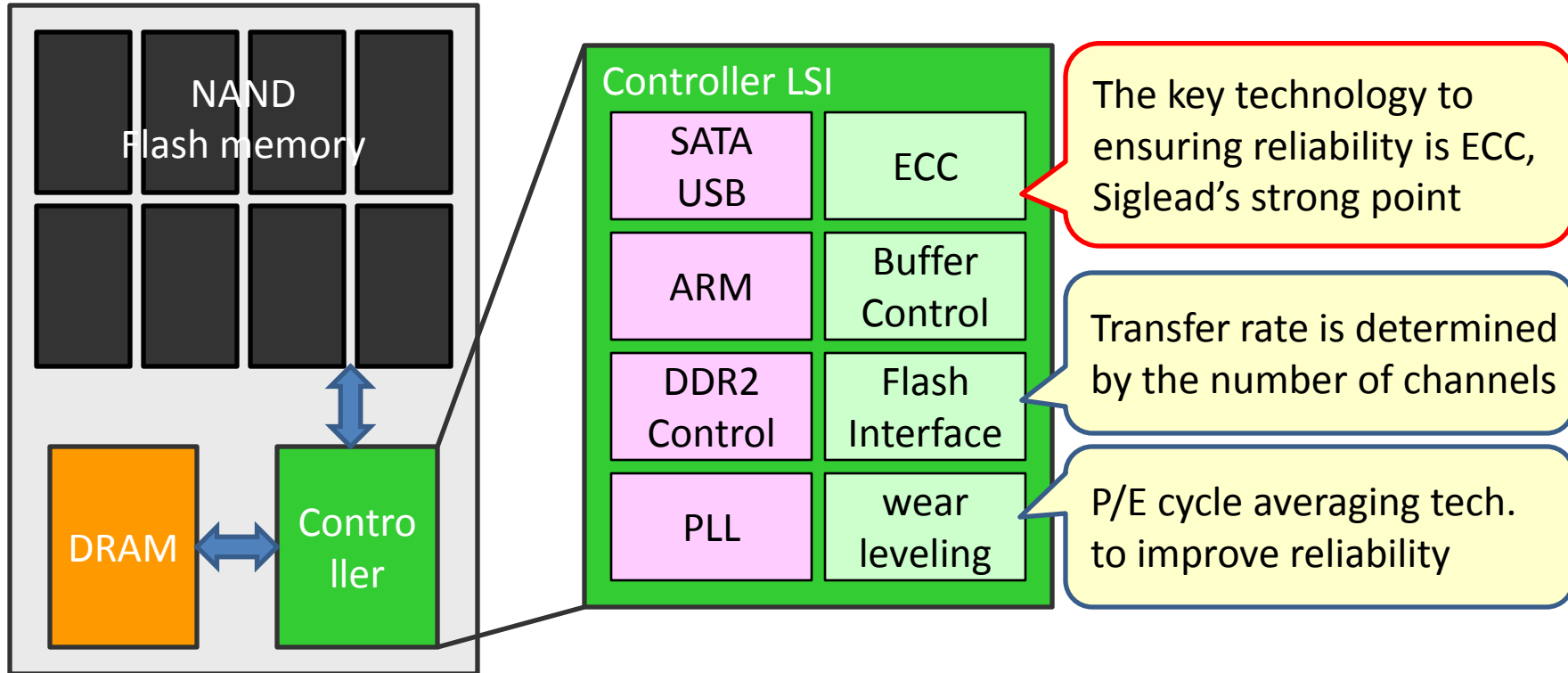
- NAND flash memory's low price is achieved by process and MLC
- However, reliability (endurance & data retention) degrades



High reliability can only be achieved by high performance controller !

SSD's Developing Trends 2 (Controller)

SSD has simple architecture. The controller plays the key role in competition

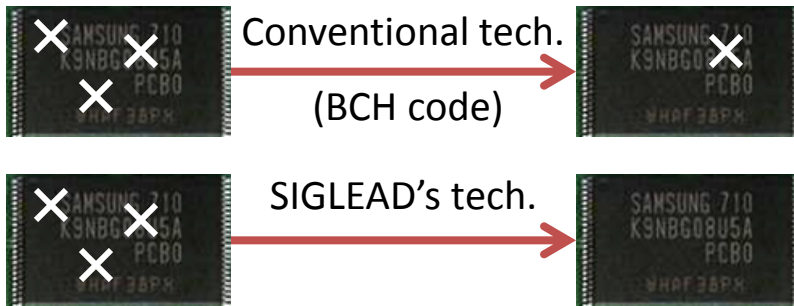


Signal processing will play an important role in improving the reliability of NAND flash memory, hence it can be empowered by Siglead's technology

Original Technology

Error number significantly reduced due to Siglead's original technology

➤ Conventional NAND flash memory

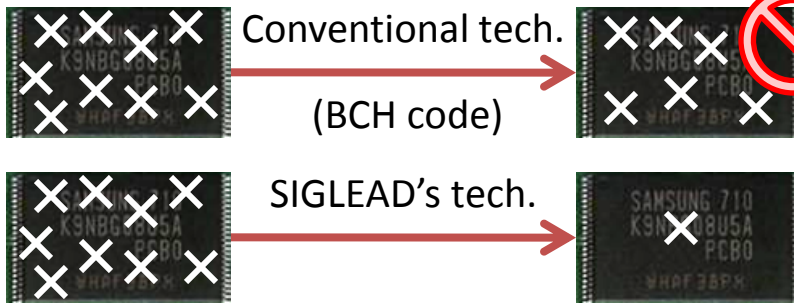


High reliability SSD



For automobile and medical equipment

➤ Minute process / MLC NAND flash memory



Fail in practical use...

Low cost SSD

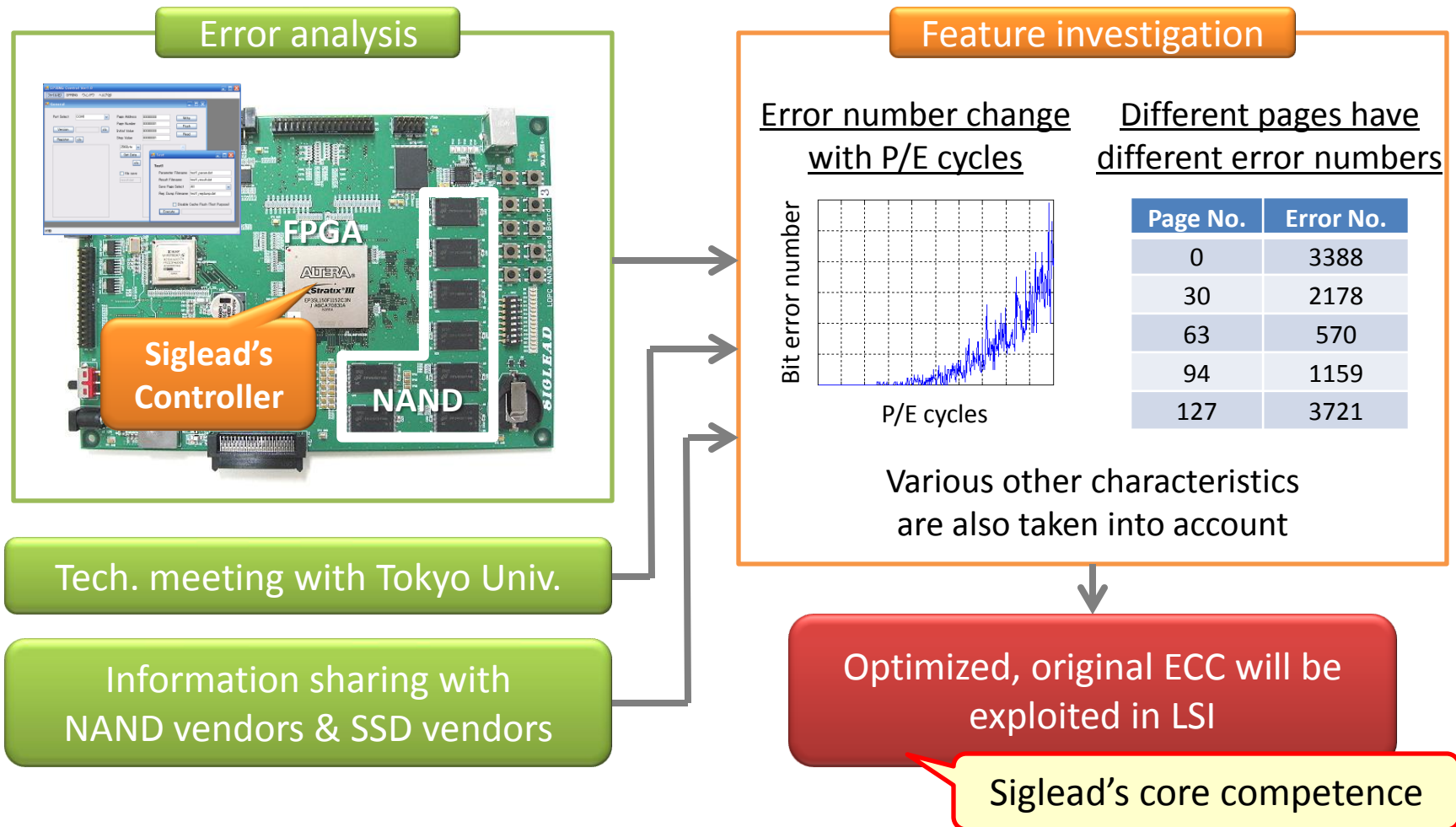


For PC and IT appliance

Low reliability NAND flash memory can be used in SSD

Original Technology

Optimized ECC construction based on error analysis

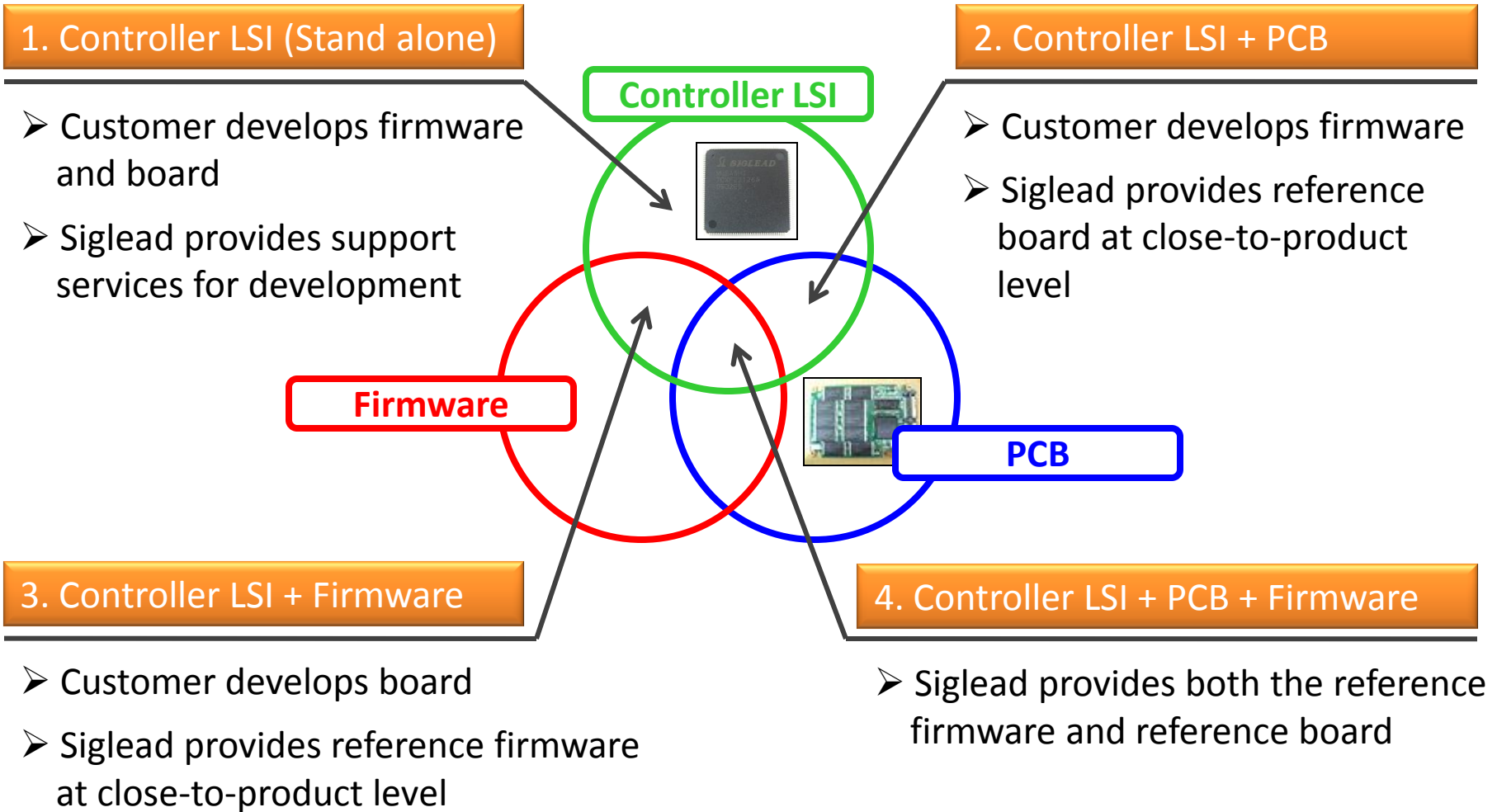


LSI Function Overview

Feature : High Speed (16channel, SATA III), High Reliability (Original ECC)

Name	SPRING		SCREW
Process	65nm LP		65nm LP
Channel	8	16	16
Package	289pin BGA	529pin BGA	529pin BGA
Sequential Read	300MB/s	500MB/s	500MB/s
Sequential Write	270MB/s	450MB/s	450MB/s
Random Read	80MB/s	T.B.D	Faster than SPRING
Random Write	50MB/s	T.B.D	Faster than SPRING
Cache	1 st sample : DDR2 Max.256MB 2 nd sample : DDR3 Max.256MB		DDR3 Max.512MB
Host I/F	SATA III (6.0Gbps)		SATA III (6.0Gpbs)
ECC	BCH with SIGLEAD original technology		SIGLEAD original
Wear Leveling	dynamic / static		dynamic / static
CPU	32bit RISC		32bit RISC
Schedule	1 st sample : 2010/10 2 nd sample : 2011/09		T.B.D

Service Options

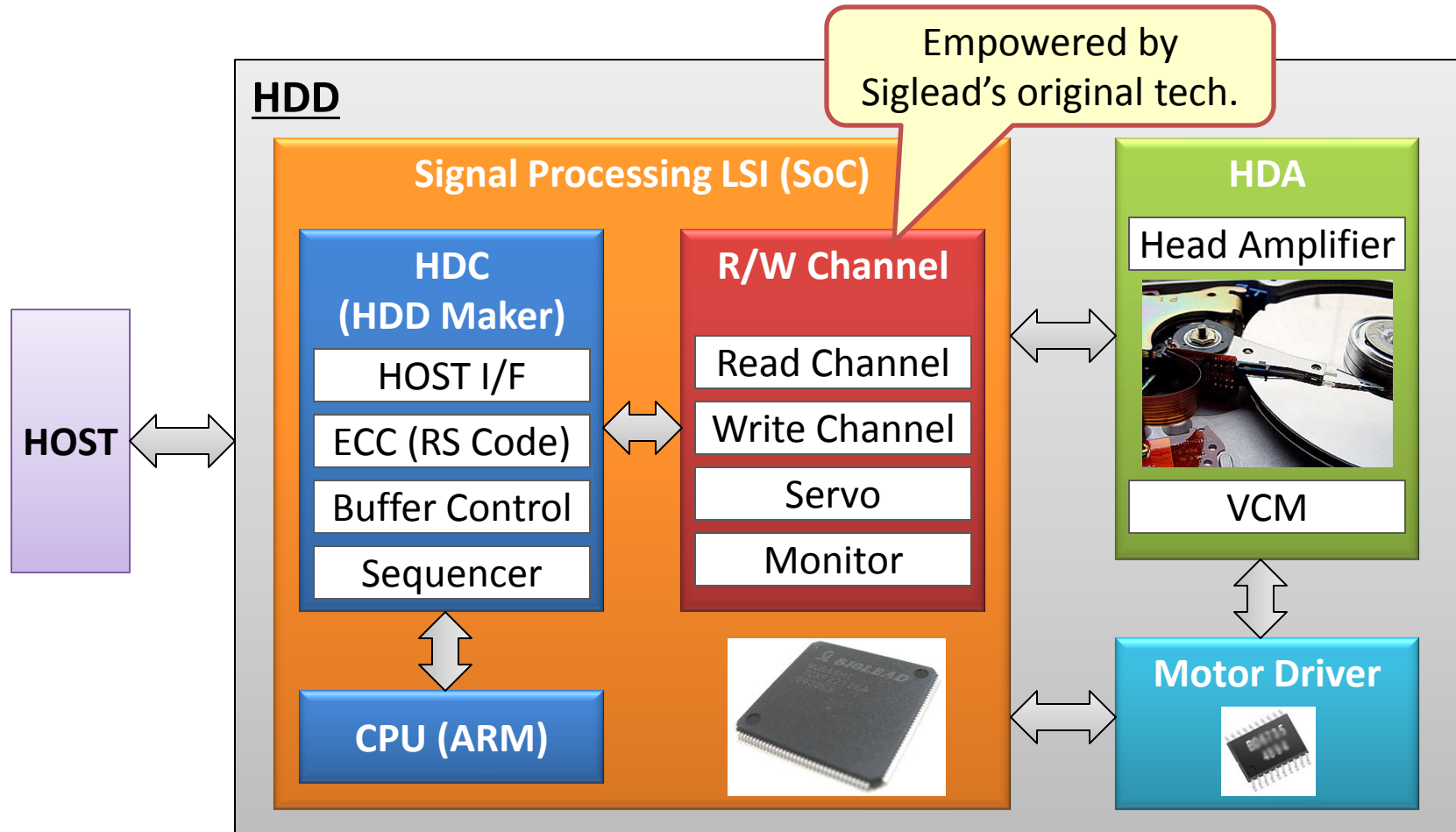


3. HDD Signal Processing LSI

Developing Target / Original Technology / New Technology

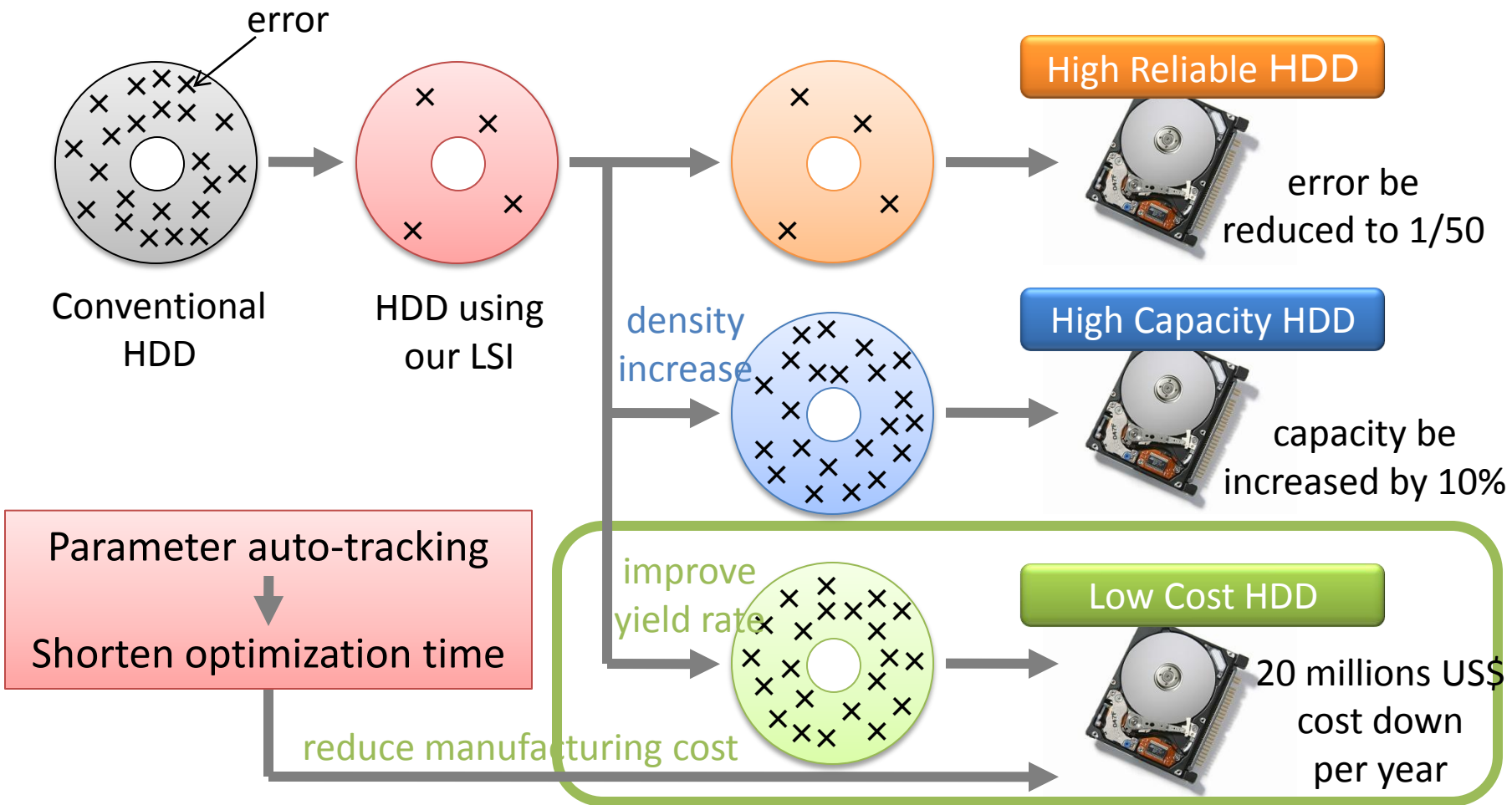
Developing Target

Focus on LSI for 2.5inch HDD, the leading power of growth



Original Technology

Significant error reduction achieved by SIGLEAD's innovation.

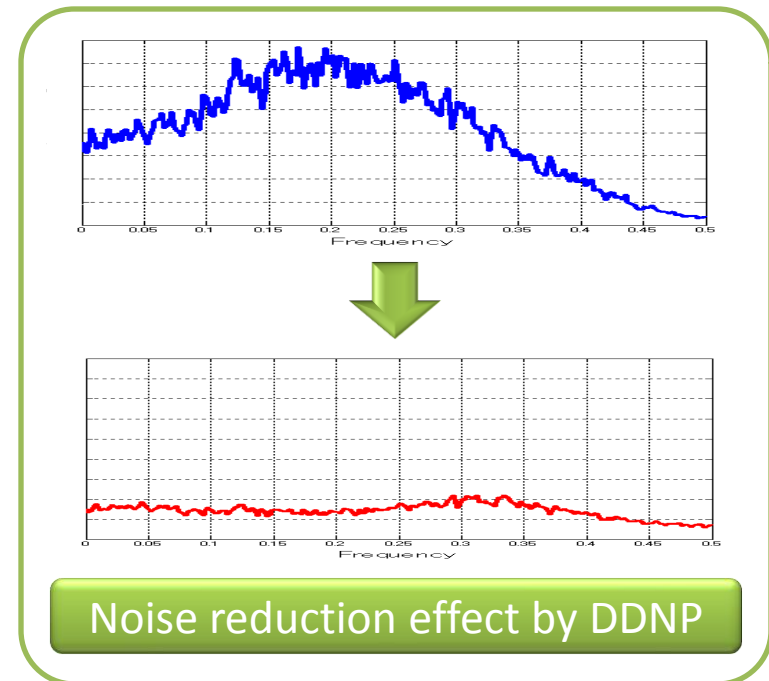
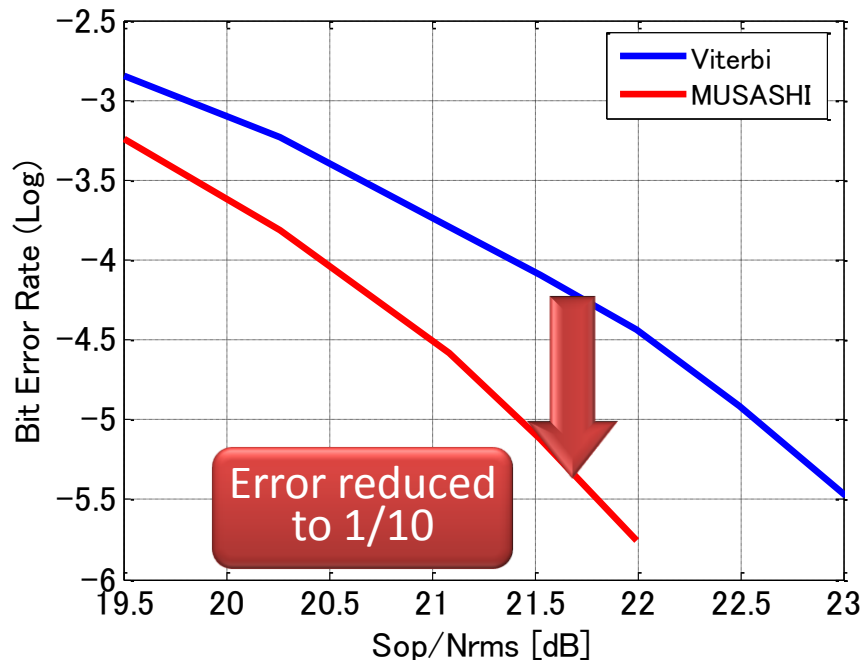


New Technology Example : Improved DDNP

DDNP (Data Dependent Noise Prediction)

Current noise prediction given by data pattern and the past noise

- Based on DDNP, improvement of channel gain and reduction of silicon size are achieved at the same time.
- Parameter auto-tracking for the environmental change is adopted.



4. Other Products

NAND Analyzer System / NAND Error Analysis Report
Signal Processing IP / FPGA Evaluation Board

NAND Analyzer System (SigNAS)

Catalog is available on our website.
<http://www.siglead.com>

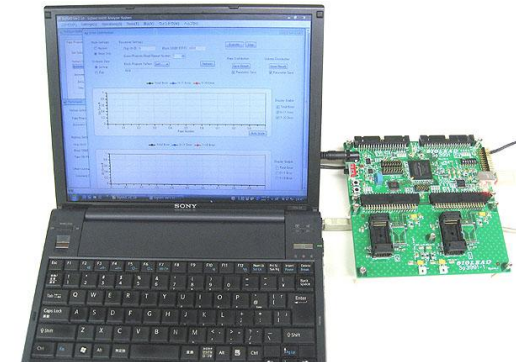
Operation verification of NAND flash memory from various vendors, error analysis, detailed error cause analysis, measurement of ECC performance, etc. can be easily done using this analyzer system.

Capability of analysis software include, but are not limited to:

- Error rate measurement (Bit error rate, Page error rate after ECC)
- Measurement of Data Retention, Program Disturb, Read Disturb
- Analysis of error distribution (Page dependence, Column dependence)
- Program pattern setting (Increment, Pseudo Random, Page Stripe, etc.)
- NAND access time measurement
- Script execution to enable flexible measurement

< Deliverable >

- Mother board, Daughter board
- Analysis software
- NAND Controller and Firmware (implemented on mother board)
- Operation manual



NAND Error Analysis Report

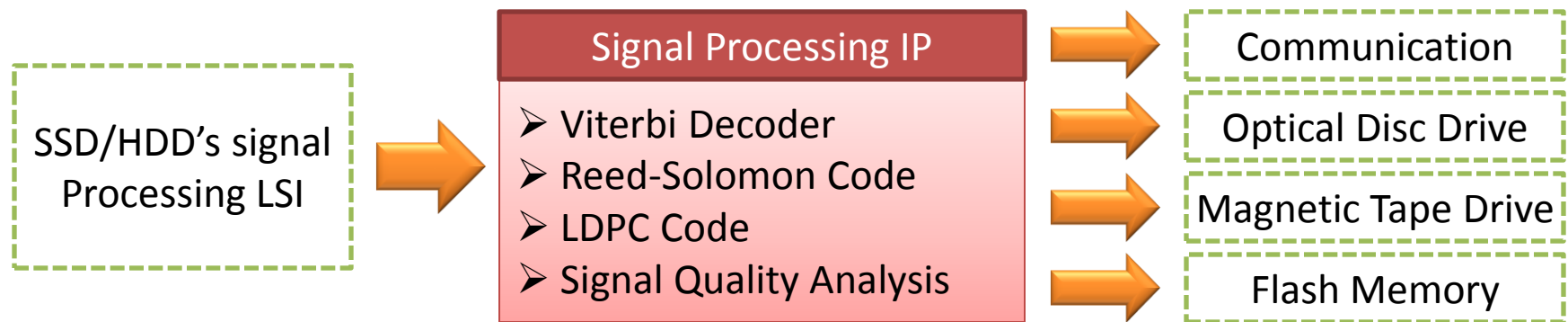
Error analysis report for customer-specified NAND flash memory

An example of deliverable report

- Various error statistics
- Data Retention measurement result (Time vs Bit error number)
- Program Disturb measurement result (P/E cycle vs Bit error number)
- Read Disturb measurement result (Read times vs Bit error number)
- Error distribution (Page dependence, Column dependence)
- Performance of error correcting code (ECC)
- NAND access time measurement result

Signal Processing IP Overview

Signal Processing IP based on the development of SSD/HDD signal processing LSI
Widely applicable to communication, optical storage and flash memory etc.



< Deliverables >

Several kinds of deliverables can be provided to meet customer's request

1. RTL Source Code
2. FPGA Netlist
3. ASIC Netlist
- etc.

Besides IP customization and peripheral circuit design, we can provide such services as optimization of user-environment-matched signal processing.

Signal Processing IP List 1

Catalog is available on our website.
<http://www.siglead.com>

1. Viterbi Decoder / Viterbi Detector

1-1. High-speed Soft Decision Viterbi Decoder

- Simplified ACS loop for high-speed design
- Convolutional code parameter configurable
- Traceback length configurable (dynamically change available)
- Support soft-output
- Option of enable/disable external memory selectable

1-2. Radix-16 High-speed Viterbi Detector

- Radix-16 and simplified ACS loop for high-speed design (2Gbps@TSMC65nm)
- Partial Response transfer function configurable
- Available two type : small-size / high-speed

1-3. Viterbi Decoder (Detector) with capability of noise prediction

- Error reduction achieved by DDNP (Data Dependent Noise Prediction)

1-4. Viterbi Decoder (Detector) with capability of distortion compensation

- Error reduction achieved by signal distortion compensation

Signal Processing IP List 2

Catalog is available on our website.
<http://www.siglead.com>

2. Reed-Solomon Code

2-1. High-speed Reed-Solomon Codec

- High-speed encoding / decoding (4bit symbol : 3.2Gbps, 8bit symbol : 2Gbps)
- RS parameters configurable (symbol, code length, information length)
- Primitive polynomial and generator polynomial configurable
- Support erasure correction

2-2. Reed-Solomon Codec Generator

- RTL, test bench and test pattern generation corresponding to our IP (2-1)

Other IP

3-1. LDPC Encoder / Decoder

3-2. BCH Encoder / Decoder

3-3. High Code Rate RLL, DC-free, MTR Encoder / Decoder

3-4. Iterative Decoder

4-1. Signal Quality Analysis : Error Rate(after ECC) Estimation Technology

5-1. Statistic-based Signal Distortion Compensation

Catalog is available on our website.
<http://www.siglead.com>

FPGA Evaluation Board Overview

- Original FPGA board with high-speed AD/DA is developed and on sale.
- Suitable for high-speed signal proc., wireless communication and image proc..

FPGA	Altera StratixIII, StratixIV (Xilinx Virtex-5 version is under planning)
ADC	12bit 550Msps 2channel
DAC	16bit 1Gsps 2channel
Memory	DDR2 SDRAM 240pin DIMM (Max 4GByte) 64MByte NOR Flash Memory
I/F	DVI Input/Output : Max UXGA (165MHz) Gigabit Ethernet Controller : PCI Bus Connection USB2.0 : A Connector x 2, miniAB Connector x 1 LVDS Connector : Input 10pair, Output 10pair (Max 10Gbps) USB Serial I/F 80pin Connector for Another Board : 40pin for User

Customization is also available.

[Customization example]

- 8bit 3Gsps ADC - 12bit 1Gsps ADC 8channel - 14bit 2.4Gsps DAC 4channel

FPGA Evaluation Board Product Picture

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